



Participant Profile

for the
Turkish-German Strategy Workshop 2006
TÜBİTAK Marmara Research Center,
Istanbul- Gebze Turkey
13 – 15 December 2006



International Bureau (IB)
of the Federal Ministry of
Education and Research
(BMBF)

1. Contact details and personal information

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¹ **Role/function** e.g. working group leader, managing director, postdoc, PhD etc.

² **Organisation type** e.g. university, research institution, small and medium enterprise (SME), industry etc.

Working Group:	<input type="checkbox"/> 1 Material Technologies <input type="checkbox"/> 2 Biotechnology, Genomics and Food <input type="checkbox"/> 3 Energy <input checked="" type="checkbox"/> 4 Information and Communication Technologies <input type="checkbox"/> 5 Environmental Protection, Climate Change and Sustainable Development	
Areas of activity:	<input checked="" type="checkbox"/> research <input type="checkbox"/> technology development <input type="checkbox"/> demonstration	<input type="checkbox"/> training <input type="checkbox"/> dissemination <input type="checkbox"/> other:
Keywords characterising your area of research:	Please choose the appropriate key words (max. 5) from the following list: http://www.cordis.lu/fp6/keywords Electronic engineering, Microelectronics, Mixed-signal design	



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**Expertise,
technologies and
infrastructures
available in your
institution:**

Research activities / expertise: electronic design automation for analog circuits, yield optimization, design centering, robust design, analog test

Methods: mathematical methods, software algorithms

Key technologies: analog optimization, layout synthesis, test generation, logic simulation, logic optimization

Infrastructures: ca. 60 workstations, High-Speed-Intranet, Leibniz-Rechenzentrum,

Key publications: J. Zou, D. Mueller, H. Graeb, U. Schlichtmann, A CPPLL Hierarchical Optimization Methodology Considering Jitter, Power and Locking Time, ACM/IEEE Design Automation Conference (DAC), 2006.
D. Mueller, G. Stehr, H. Graeb, U. Schlichtmann, Deterministic Approaches to Analog Performance Space Exploration, ACM/IEEE Design Automation Conference (DAC), 2005.
G. Stehr, H. Graeb, K. Antreich: Analog Performance Space Exploration by Fourier-Motzkin Elimination with Application to Hierarchical Sizing, IEEE International Conference on Computer-Aided Design (ICCAD), 2004.
G. Stehr, M. Pronath, F. Schenkel, H. Graeb, K. Antreich: Initial Sizing of Analog Integrated Circuits by Centering within Topology-Given Implicit Specifications, IEEE International Conference on Computer-Aided Design (ICCAD), 2003.
G. Stehr, H. Graeb, K. Antreich: Performance Trade-off Analysis of Analog Circuits By Normal-Boundary Intersection, ACM/IEEE Design Automation Conference (DAC), 2003.
H. Graeb, S. Zizala, J. Eckmueller, K. Antreich: The Sizing Rules Method for Analog Integrated Circuit Design, IEEE International Conference on Computer-Aided Design (ICCAD), 2001.
M. Pronath, H. Graeb, K. Antreich: On parametric test design for analog integrated circuits considering error in measurement and stimulus, Int. Series of Numerical Mathematics, Vol. 146, 2003.
G. Stehr, H. Graeb, K. Antreich: Feasibility regions and their significance to the hierarchical optimization of analog and mixed-signal systems, Int. Series of Numerical Mathematics, Vol. 146, 2003.
K. Antreich, H. Graeb: Circuit optimization driven by worst-case distances, In: The Best of ICCAD - 20 Years of Excellence in Computer-Aided Design, Kluwer Academic Publishers, 2003.
W. Lindermeir, H. Graeb, K. Antreich: Analog Testing by Characteristic Observation Inference, IEEE Transactions on Computer-Aided Design of Integrated Circuits (CAD), 1999.
W. Lindermeir, H. Graeb: On the production test of analog circuits by statistical fault modeling, AEÜ International Journal of Electronics and Communications, 1995.
K. Antreich, H. Graeb, C. Wieser: Circuit analysis and optimization driven by worst-case distances, IEEE Transactions on Computer-Aided Design of Integrated Circuits (CAD), 1994.
K. Antreich, H. Graeb, R. Koblitz: Advanced yield optimization techniques, in: Advances in CAD for VLSI 8 (Edts. Director, Maly), Kluwer Academic Publishers, 1994.
K. Antreich, H. Graeb, C. Wieser: Practical methods for worst-case and yield analysis of analog integrated circuits, International Journal of High Speed Electronics, 1993.



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2. Past and present research collaborations

Are you familiar
with the European
Framework
Programme?

Yes

No

- with Framework Programme 5
- with Framework Programme 6
- with Framework Programme 7

EU-projects you are
involved in:
Past projects

**Programme title / contract number / title / acronym / your function
(coordinator / partner / contractor)**

Present projects

(FP6-Antrag 035121 NEADA)

Other international
collaborations:

Carnegie Mellon University, Prof. Rutenbar,
Katholieke Universiteit Leuven, Prof. Gielen,

Name(s) and
contact details of
potential partners:

**If you would like to suggest the participation of particular partners from the
partner country based on existing contacts or collaboration experience,
you are welcome to indicate their names and contact details below:**

Prof. Günhan Dündar, Bogazici University, Istanbul, dundar@boun.edu.tr

3. Presentation at the Workshop

I will give a presentation at the workshop (approx. 10 min.) to present my institution, my expertise, and my collaboration interests. The contents of my presentations is summarised below (max. 1 page).

The research projects of the Institute of Electronic Design Automation (Prof. Schlichtmann) are dedicated to develop and provide methods and tools that support the designer in industry with computer aids in his daily circuit and system design tasks.

The 1999 edition of the Technology Roadmap for Semiconductors of the Semiconductor Industry Association (SIA) reports that a growth rate of 60% per year in system complexity faces a growth rate of only 20% per year in design productivity. The editors conclude that design productivity by electronic design automation has to be increased drastically, in order to be really able to benefit from the progress in semiconductor technology.

This means an ongoing great demand for know-how in the areas of design & test, which is a real challenge considering that the design of systems and system components - and, consequently, the design automation - is a key issue of electrical and electronics engineering.

The research program of the Institute of Electronic Design Automation covers a broad range of computer-aided design techniques for digital and analog circuits. The large depth of own research activities across all levels of abstraction - from the architectural level across the logic and circuit level to the layout level - meets the requirements of solving some of the difficult design tasks mentioned in the Roadmap.

I agree with the publication of my data on the Workshop website!

PLEASE FILL IN THIS FORM UNTIL 22 SEPT. 2006 AND RETURN IT TO:

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Christian.schache@dlr.de

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